Notice of Allowability	Application No.	Applicant(s)	
	10/032,465	MORI ET AL.	
	Examiner	Art Unit	
	Daniel D. Chang	2819	
The MAILING DATE of this communication appears on the cover sheet with the correspondence address All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS. This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.			
1. This communication is responsive to <u>application filed 1/2/2002</u> .			
2. The allowed claim(s) is/are <u>1-16</u> .			
3. The drawings filed on <u>02 January 2002</u> are accepted by the Examiner.			
 4.			
Attachment(s) 1. ☑ Notice of References Cited (PTO-892) 2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948) 3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/0 Paper No./Mail Date 4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material	5. Notice of Informal Pa 6. Interview Summary (Paper No./Mail Date 8), 7. Examiner's Amendm 8. Examiner's Statemen 9. Other	(PTO-413), e nent/Comment	
		Daniel D. Chang Primary Examiner Art Unit: 2819	

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Priority

Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Japan on 5/25/2001. It is noted, however, that applicant has not filed a certified copy of the JAPAN 2001-156687 application as required by 35 U.S.C. 119(b).

Reasons for Allowance

Claims 1-16 are allowable over the prior art of record.

The following is an examiner's statement of reasons for allowance: the best prior art of record, Ooishi, taken alone or in combination of other references, does not teach or fairly suggest a semiconductor integrated circuit comprising, among other things, an internal power supply line for connecting to each other said power supply terminals of said first circuit blocks operating at different timings among said first circuit blocks; and a power supply control circuit for simultaneously turning on said switching transistors connected to said internal power supply line, in response to operation(s) of at least any one of said first circuit blocks connected to said internal power supply line, as set forth in the claim.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

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Contact Information

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel D. Chang whose telephone number is (571) 272-1801. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J. Tokar can be reached on (571) 272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Daniel D. Chang Primary Examiner Art Unit 2819

DANIEL CHANG PRIMARY EXAMINER

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